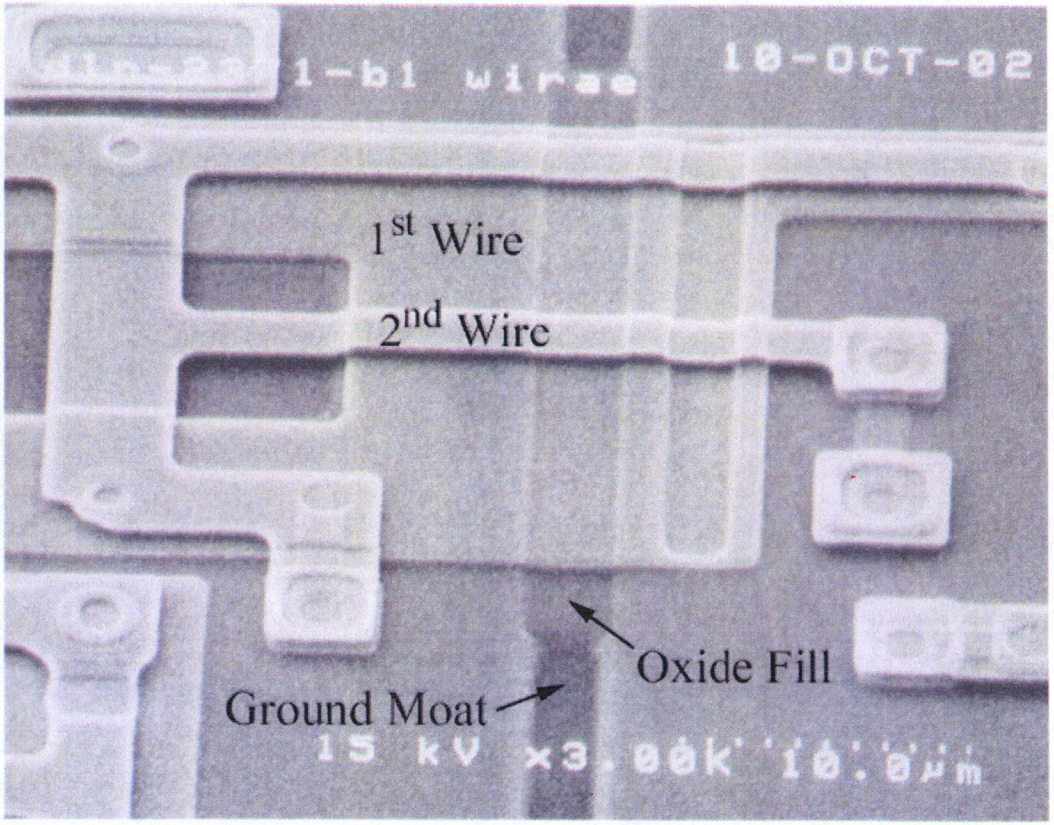
P13

Josephson Junction Circuit

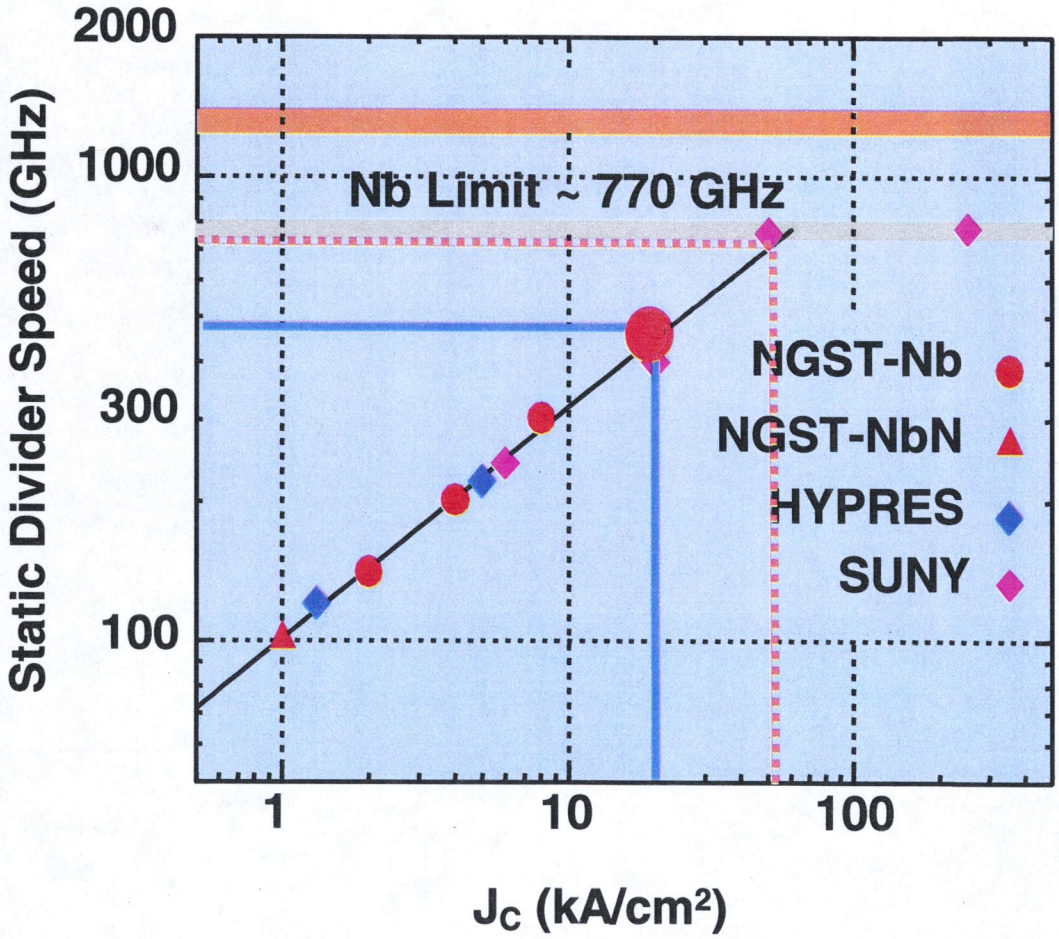


SEM picture of first and second wiring layers crossing ground moat filled with oxide.

P54

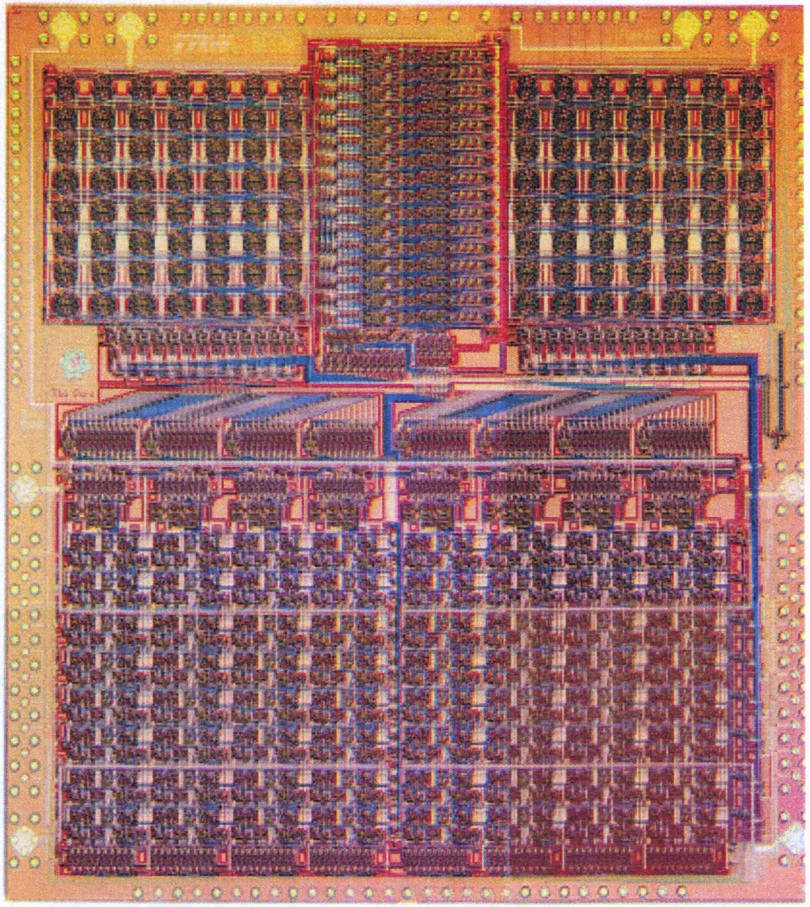
STA

Static Divider Speeds



FLUX-1R1 Chip

Source: **2002 NGST/SUNY-Stony Brook/JPL**



Fabricated in NGST process:

- 4 kA/cm2
- 4 superconductor layers
- 8-bit scalable microprocessor prototype
- Contains 63K JJs
- 10.3x10.6-mm chip
- Designed to operate at 20 GHz
- Scan path testing is incomplete

P19

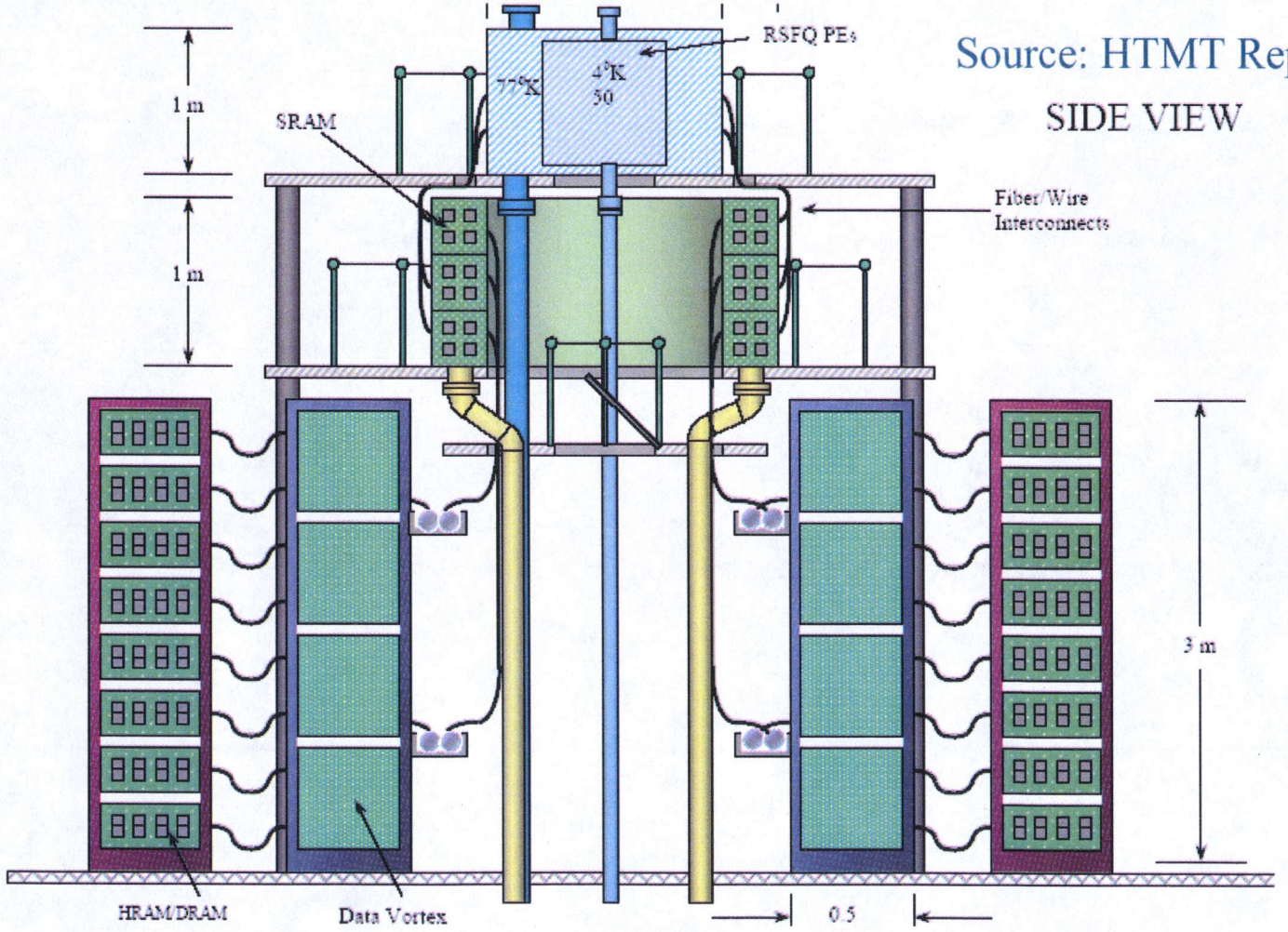
STA

Japanese Petaflops System Proposal

Japanese Petaflops Project Targets (as proposed at the end of 2004)	
Die size	1 cm x 1 cm
Fabrication process	0.25 µm, 160 kA/cm^2 Nb process
Processor clock	100 GHz
Processor performance (peak)	100 GFLOPS
On-chip processor cache	256KB
Off-chip memory per processor	32 MB hybrid SFQ-CMOS
Number of system nodes (8 CPUs per node)	2,048
Intra-node processor-memory bandwidth (peak)	800 GB/sec
Total DRAM memory at 77 K	200 TB (100GB/node)
Total number of processors per system	16,384
System Performance (peak)	1.6 petaflops
Power at the 4.2K stage	18 kW
Power of the cryocooler	12 MW

P22

Concept for a Large Scale System



Source: HTMT Report

SIDE VIEW

Technical Issues

- Providing high speed, low latency memory
- Architecting systems that tolerate significant memory access latencies
- Providing very-high-data-rate communications into and (particularly) out of the cryogenic environment
- Low Risk Technical Issues:
  - Providing powerful CAD tools for the designers
  - Achieving a stable fabrication process
  - Refrigeration

Roadmap Created

Tools and components essential for RSFQ-based high-end computing by 2010. End points include:

- An RSFQ processor demonstration
  - 1 M gates
  - 50 GHz clock
- A design capability
  - Cell library and complete suite of CAD tools
  - Allowing a competent ASIC digital designer with no background in superconductor electronics to design high performance chips
- Established RSFQ chip manufacturing

P25

Superconductor circuit technology readiness

Circuit Type	2004 Readiness	Projected 2010 Readiness
Logic	Small circuits at lower speed	> 10^6 JJ/cm^2 at 50 GHz clock
SFQ RAM	Experimental 4K RAM at low speed Analysis of SFQ ballistic RAM	256 kbit SFQ ballistic RAM at 500 ps
Hybrid RSFQ-CMOS RAM	Experimental proof-of-concept	256 kbit hybrid at 500 ps
Monolithic RSFQ MRAM	RSFQ write/read concept formulated	128 kb hybrid at 500 ps
Vector Register, FIFO	32 bit FIFO at 40 GHz	4 K FIFO at 50 GHz
Communication Circuits	Chip-to-chip at 60 Gbps	64-bit word-wide chip-to-chip at 50 GHz
I/O	10 Gbps driver	64-bit word-wide drivers at 40 Gbps/s
Switch	2.5 Gbps per port circuit switch, scalable	64-bit word wide, scalable at 50 Gbps per port

Superconductor circuit technology is ready for major investment and development.

RSFQ Technology Is Viable

RSFQ in a Nutshell	
Technical Advantages	**Technical Challenges**
The most advanced alternative technology	Providing high speed and low latency memory
Combines high speed with low power	Architecting systems that can tolerate significant memory access latencies
Ready for aggressive investment	Providing very high data rate communications between room temperature technology and cooled RSFQ